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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/774,933	
	Filing Date	February 9, 2004	
	First Named Inventor	Guen-Hee CHO	
	Art Unit	2816	
	Examiner Name	Cassandra F. Cox	
Total Number of Pages in This Submission	3	Attorney Docket Number	8021-202 (SS-19131-US)

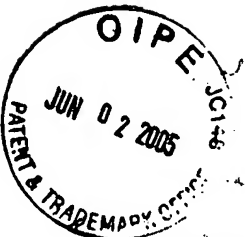
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Richard D. Ratchford Jr., Reg. No. 53,865, F.Chau & Associates, LLC
Signature	
Date	5/31/05

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Guen-Hee Cho

DOCKET: 8021-202 (SS-19131-US)

SERIAL NO.: 10/774,933

GROUP ART UNIT: 2816

FILED: February 9, 2004

EXAMINER: Cox, Cassandra F.

**FOR: DELAY-LOCKED LOOP (DLL) CAPABLE OF DIRECTLY
RECEIVING EXTERNAL CLOCK SIGNALS**

Commissioner for Patents
P.O. Box 1450
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RESPONSE TO RESTRICTION REQUIREMENT

Sir:

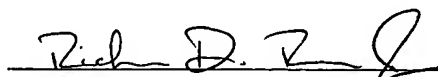
In response to the Office Action dated May 6, 2005, Applicants provisionally
elect the claims of Group I (i.e., claims 1-25) with traverse.

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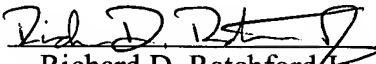
5/31/05


Richard D. Ratchford Jr.

While the devices of Groups I and II may be distinct as set forth by the Examiner, Applicants believe that simultaneous examination will not present an undue burden. For example, the claims of Group I are drawn to a delay locked loop including, inter alia, an internal clock signal generator, classified in class 327, subclass 147 and the claims of Group II are drawn to an internal clock signal generator, classified in class 327, subclass 291. Under such circumstances, the Examiner is encouraged to maintain the claims of Groups I and II in the same application. See, MPEP § 803.

Early and favorable consideration of the application is earnestly solicited.

Respectfully submitted,

By: 
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